PATENT CLAIMS

1. Method to produce an insulated gate semiconductor device cell, comprising the steps of

   - forming a cell window (3) in a layered structure (2) on a cathode side of a semiconductor substrate (1), said layered structure comprising an oxide layer (22) on top of said semiconductor substrate (1) and a poly-silicon layer (21) on top of said oxide layer (22),
     said cell window being formed by partially removing said layered structure down to the substrate, leaving at least two isolated strips (41, 42) of the layered structure to remain within the cell window,
     said isolated strips (41, 42) dividing the cell window (3) in an outer cell window region located between the isolated strips and the outer edge of the cell window and an inner cell window region located between the isolated strips;
   - forming doped regions (11, 12) in the semiconductor substrate by applying a process mask to the inner or outer cell window region respectively and implanting dopants into the substrate through the other, uncovered cell window region;

   characterized in, that

   - in or after the cell window forming step, openings (411, 421) in the isolated strips (41, 42) are formed by further removing some of said layered structure down to the substrate, and that
   - a doped region (13) in the semiconductor substrate beneath the openings (411, 421) is formed by implanting dopants into the substrate through the openings (411, 421).

2. An insulated gate semiconductor device, comprising

- a layered structure (2) on an essentially planar cathode side of a semiconductor substrate (1), said layered structure being arranged around a cell window (3) and forming an insulated gate comprising an oxide layer (22) on top of said semiconductor substrate (1) and a poly-silicon layer (21) on top of said oxide layer (22),
- a first doped region (11) of a first conductivity type extending into the substrate beneath the centre of said cell window (12),
- a second doped region (12) of a first conductivity type, in particular a shallow base region (12), extending into the semiconductor substrate beneath the outer edge of the cell window adjacent said first doped region (11);
- at least one third doped region (13) of a second conductivity type, in particular a source region (13), extending partially into said second doped region (12) adjacent said first doped region (11); and
- a first main contact (6) disposed on the top surface electrically connected to said first doped region (11) and said third doped region (13);

characterized in that

- at least two isolated strips (41, 42) are arranged in the cell window (3) between the insulated gate (21) and the first main contact (6), dividing the cell window (3) in an outer cell window region and an inner cell window region, said outer cell window region being located between the isolated strips and insulated gate (21) and above the third doped region (13), and said inner cell window region being located between the isolated strips and comprising the main contact (6),
  said strips comprising an oxide layer on top of the semiconductor substrate and a poly-silicon layer on top of the oxide layer, that
- the two strips comprise openings (411, 421), and that
- the third doped region (13) extends into the substrate beneath the openings, electrically connecting the third doped region (13) beneath the outer cell window region to the first main contact (6).

3. An insulated gate semiconductor device as in claim 2, characterized in, that

   - the ratio length of openings (411, 421) to lengths of strips is laid out to match a desired emitter ballast resistance.